MULTIChip MODULES

Don W. Baudrand and N.V. Mandich

ABSTRACT

Electronic devices made using ceramic substrates are increasing in use in popularity because ceramics provide stability and strength. A few examples are: hybrid circuits, multilayer ceramic circuits, connectors, tube bases, capacitors, and chip carriers. These devices often require electroplating at some point in the fabrication process. Some successful procedures for cleaning, preparing and electroplating the metallized areas are detailed in this paper.

INTRODUCTION

A firmly entrenched and growing for producing circuits and chip carriers is the use of ceramic microelectronic technology. Instead of a copper clad substrate for the printed circuit, ceramic based materials are used. Chips and other discrete components can be mounted directly onto the surface of metallized ceramic substrates rather than pin mounted in plated through holes. Although surface mounting of devices is also used on PC boards, ceramic hybrids offer a number of advantages that make their use more attractive and in some cases mandatory. Among these are miniaturization, reliability, thermal shock resistant, the ability to be cut and drilled to extremely fine tolerances, ease of multi-layer manufacture and favorable dielectric constants.

CERAMIC PACKAGING

The functions performed by a section of a PC board, or one or more entire boards, can be condensed into a single small and highly reliable unit using ceramic technology. Hybrids can be mounted onto PC boards to perform their circuit functions, or in some applications can be used as a complete self-contained electronics package. Figure 1 shows several typical hybrids with their package lids removed. The item in the lower left corner of figure 1 is a metallized ceramic substrate. Item in the lower right-hand corner of Figure 1 is a similar substrate after component mounting, wire bonding and packaging. Figure 2 shows the component placement and circuit layout of the first substrate. Comparing this to printed circuit boards, all chips would be mounted in dual inline packages (DIP'S) or similar packages, along with resistors, capacitors and other components. The second substrate is a similar substrate after component mounting and soldered in place. Miniaturization and reliability are made possible using multi-layer ceramic designs.

Although the tight assembly tolerances of miniaturized hybrids require delicate manual component placement of expensive automated precision pick-and-place assembly machines, the elimination of lead mounting greatly increases circuit reliability. The sealed hybrid package is not subject to failure because of mechanical stress on component leads during manufacture, handling, or operation. Hybrids can also withstand greater thermal, vibration and mechanical shock than PS boards.

Figures 3 and 4 show two typical methods of automated component placement: the vacuum stylus and tweezers grippers. Figure 5 shows an IC chip that has been die bonded to the substrate and connected to external circuitry by wire bonding. Components are often mounted into metallized areas of the ceramic using a conductive epoxy or paste. Die bonding is also often achieved using a gold/silicon eutectic perform that is brazed by heating. Wire bonding is achieved by applying thermosonic, thermo compression, or ultrasonic energy to the wire ends so that they deform plastically and bond to metallized pads. Soldering is also used to mount components and connect them.

Electroless nickel (EN) deposits, especially electroless nickel-boron deposits, can produce a surface with the characteristics necessarily to achieve mounting and connection of components. Most electroless nickel-boron deposits are solderable, brazable, and can be wire bonded most, but not all, epoxy bonding materials adhere to these deposits as well. The authors prefer amine-hardened epoxies. Electroless nickel deposits provide the needed corrosion protection for molybdenum and molybdenum manganese metallizing frits. They also provide conductivity improvement for these and other metallizing materials such as tungsten. These materials are selected because they most closely match the coefficient of expansion of ceramic substrate materials such as 96% alumina. Mixing and firing procedures are found in references 3, 4 and 6.

Aluminum wire can be bonded to nickel-boron deposits using ultrasonic of thermosonic methods, but cannot be bonded with thermocompression methods. Gold wire can be bonded to Ni-B only by thermosonic techniques. Some electroless nickel-phosphorus deposits with high phosphorus, 10-11%P by wt, can also be wire bonded using these techniques. However, it seems to be more difficult to find the correct operating conditions of temperature and energy level to use in bonding. Wire bonding to electroless nickel requires higher ultrasonic energy (more pressure) than bonding to gold. Metallized refers to conductive mounting pads and circuit traces that have been silk-screened
Ceramic materials are provided as powders that are slurried, binder and the mixing and firing conditions can create porosity in alumina that promotes good adhesion to electroless plating processes. Higher purity alumina, the 96% purity grade is proffered because it can be made to be less reactive to the electroless nickel plating process. Alumina is the most commonly used. It is available in purities of 94%, 96%, 99% and 99.5%. When electroless nickel will be plated directly onto alumina, the 96% purity grade is proffered because it can be etched with fluoride containing acid to produce a microporous, hydrophilic surface that promotes good adhesion to electroless plating processes. Higher purity alumina does not etch well in fluoride etchants. Careful selection of binder and the mixing and firing conditions can create porosity in alumina.

Ceramic materials are easily machined, drilled and punched to tight tolerances in both the relatively soft uncured state, called the "green state" and in the final fired or cured state. Ceramic materials contract about 17% during firing, so machining and punching operations performed prior to firing must take this shrinking into consideration and must adjust the dimensions accordingly. The cured ceramic is easily cut and drilled by laser machining for precision. Through-holes and circuitry can even be added after fabrication by these methods to alter or customize.

Another advantage of hybrid technology is that screening a known area of substrate with a metallizing paste of known resistance can make adequate electroplating thickness and continuity, especially in through-holes of high "aspect ratio" (smaller diameter holes).

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The thermal coefficient of expansion (TCE) of various ceramics closely matched the TCE of Kovar and other metals and alloys used in the electronics industry. This means that during "burn-in" testing or high-temperature operation of the hybrid, there will be no mechanical stress in connections or between the substrate and metallization due to mismatched thermal expansion. This provides improved component mounting and interconnection reliability in this application. In addition, reduces variations in inherent circuit capacitance that can become a design nuisance. The minimal thermal expansion also enables very fine, closely spaced circuit lines to be used without rear of failure by cracking during stress.

FABRICATION OF MULTILAYER PACKAGING

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The ease of manufacturing multi-layer circuits with ceramic materials allows complex and numerous interconnections to be made within a small area. These circuits are not easily accommodated on single-plane substrates and would require large surface area and some hard wiring. PC boards can also be multi-layered, but each layer must be manufactured and then laminated together. The thickness of multi-layer PC boards also present difficulties with plating through-holes (interconnections between board layers). These holes must be plated with a conductive material usually copper plated over electroless copper strike. The poor throwing power of the electroplating solutions may not provide adequate electroplating thickness and continuity, especially in through-holes of high "aspect ratio" (smaller diameter holes).

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These problems can be eliminated with ceramic hybrids. Ceramic layers can be formed, fired, metallized and then laminated together. Also ceramic layers can be formed, metallized and layered in the uncured state and the entire package furnace cured at the same time (co-fired). The thickness of ceramic layers is less than PC boards. The through-holes are not plated, but have metallization paste screened into them to completely fill the holes and form a solid conductor. The completed and fired multi-layer substrate contains layered layers of complex wiring, ground planes and interconnection holes in a compact package of exceptional reliability. For example, one of the simplest ceramic circuits is a chip carrier (similar to a DIP). Figure 6 shows several steps in the build-up of a slightly more complex leadless chip carrier that holds several chips and required 12 ceramic layers, including those used only for insulation. Chip carriers up to 30 layers have been fabricated in production. Should plated-through holes in multi-layer ceramics become necessary, alkaline or neutral electroless nickel-boron plating solutions can plate through very small holes. The addition of a small amount of surfactant and keeping the holes vertical during plating will allow very small gas bubbles to sweep through holes supplying fresh plating solution continuously. This results in uniform thickness in the holes and provides good electrical conductivity. Electroless nickel-boron deposits have better electrical conductivity then the metallizing materials typically used for metallization and interconnections.

Another advantage of hybrid technology is that screening a known area of substrate with a metallizing paste of known resistance can make resistors. There resistors can be laser or abrasive trimmed after manufacture to adjust to the specified tolerances. Capacitors can also be manufactured and trimmed in the same manner by applying metallization areas that are insulated by layers of ceramic dielectric or placed side by side. The dielectric constant of ceramic materials allows thinner spacing between capacitor and conductors to produce the specified characteristics in a smaller area.

MATERIALS AND PROCESSING CERAMIC SUBSTRAATES

The most common ceramic materials used for hybrid circuits and multi-chip modules are:

<table>
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<tr>
<th>NAME</th>
<th>FORMULA</th>
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<tbody>
<tr>
<td>Alumina</td>
<td>Al₂O₃</td>
</tr>
<tr>
<td>Barium titanate</td>
<td>BaTiO₃</td>
</tr>
<tr>
<td>Beryllia</td>
<td>BeO</td>
</tr>
<tr>
<td>Forsterite</td>
<td>MgO·SiO₂</td>
</tr>
<tr>
<td>Aluminum Nitride</td>
<td>AlN</td>
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</tbody>
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Alumina is the most commonly used. It is available in purities of 94%, 96%, 99% and 99.5%. When electroless nickel will be plated directly onto alumina, the 96% purity grade is proffered because it can be etched with fluoride containing acid to produce a microporous, hydrophilic surface that promotes good adhesion to electroless plating processes. Higher purity alumina does not etch well in fluoride etchants. Careful selection of binder and the mixing and firing conditions can create porosity in alumina.

Ceramic materials are provided as powders that are slurried, formed into sheets, dried and fired at high temperature to cure and fuse into...
hybrid substrate material. The liquid ceramic is referred to as "slip" and can be cast into many shapes. It is commonly formed into a tape casting or continuous ribbon to make hybrid circuits.

**CERAMIC MANUFACTURE**

1. Vibrate the "cone-blender". Add the ceramic powder of desired purity and particle size.
2. Blend the raw materials, including plasticizers and binders.
3. Add the liquid organic vehicle (for easy pouring). De-aerate the blend.
4. Strain through a sieve to remove large particles and agglomerates.
5. Cast the slurry ("slip"); by pouring it into molds. Or by pouring at a uniform rate onto clean glass or plastic strips moving at a constant speed. Paper is sometimes used, which becomes part of the casting. The thickness is controlled by the speed of pouring, speed of the tape and by a "doctor blade" that levels the blend and removes excess slip.
6. Air dry the ceramic and remove it from the mold or backing strip. Sometimes backing is involved. The ceramic at this stage is known as "green sheet" because of its uncured state. The color is usually white. It is then cut to size; through-holes for vias are punched or drilled, and the sheets are laminated to the desired thickness. The circuit may be added in the form of the metallizing pastes.
7. The ceramic is then fired at high temperatures to produce the final form. Firing causes shrinkage, therefore all the holes and other cutting or sizzling must take into consideration the amount of shrinkage expected, usually about 17%.

**PLATING OF CERAMIC MICROELECTRONIC CIRCUITS**

Electroless nickel-boron (Ni-B) alloys are best suited for this type of circuit s. There are several types of Ni-B processes, differing slightly in deposit properties. For best soldering and wire bonding, where long shelf live before soldering is not required, low boron content alloys), 0.3-1.0% B work well. Low boron deposits have the lowest resistance (7.8 micro-ohm cm). F0r longer shelf life solderability and wire bonding, higher boron content processes are used (2-3%). Resistance ranges from 20-60 micro-ohm cm. For best overall solderability, low boron poly-alloys are suggested. All of these provide diffusion and migration barriers. All are suitable for die attachment by gold silica eutectic, or epoxy adhesive bonding. In some cases nickel phosphorus deposits can be used for these purposes. Los phosphorus deposits (4% or less) can be soldered and wire bonded. Shelf life is limited therefore soldering should take place soon after plating, or an over coating of gold can be applied. Nickel phosphorus deposits above 4% P tend to crack under brazing conditions making it difficult to achieve hermetic seals. Brazing to nickel-boron results in good hermetic seals as tested by mass spectrometer methods.

**ELECTROLESS NICKEL PLATING PROCESS CYCLES FOR METALLIZED CERAMIC DIVICES**

**Plating onto molybdenum/manganese (moly-mag)**

1. Alkaline clean. Ultrasonic cleaning can be important if there is any possibility of ceramic dust on the surface or in holes.
2. Treat to remove traces of moly-mag or moly from the ceramic surface in areas between the circuit elements. This done with a solution of 200 g/L potassium ferricyanide and 100 g/L potassium hydroxide. This is both a removal and activation step. Parts are immersed for 30-60 seconds at room temperature. Longer times or higher temperatures may result in loss of circuit dimensions. Because the ferricyanide solution is activating, it may be used again after glass removal, 10-20 seconds
3. Rinse for 1 minute with DI water.
4. Immerse in hot KOH solution to remove traces of silicon (glass) from the surface of the moly-mag. Use 100 g/L KOH at 100C (212F) to boiling for 10-15 minutes. The time is dependent on the amount of glass to be removed. Do not over etch as it may loosen the bond to ceramic. Too short a time will leave glass on the surface resulting in poor adhesion of the plated deposit. Ammonium bifluoride/hydrofluoric acid mixtures can also be used to etch glass. Caution must be used with either process. The extreme heat of the KOH solution is dangerous and the hazards of using fluorides are present in the room temperature fluoride process.
5. Rinse thoroughly with DI water.
6. Catalyze the surface for 30 seconds in a solution of palladium, silver, nickel salts or other catalytic material at room temperature. (Palladium is most commonly used.) To minimize the effect of an immersion deposit, use the lowest concentration that will provide an active catalytic surface. The actual optimum concentration varies with the condition of the metallization and must be determined experimentally.
7. Rinse with DI water.
8. Dip in 10% HCL for 30-45 seconds at room temperature.
9. Plate with electroless nickel-boron plating solution to a thickness of at least 2.5 micrometers. This minimum thickness is required to assure that enough nickel is left on the surface for tinning and chip joining after brazing. Some nickel diffuses into the molybdenum/manganese during brazing cycles of 454C to 850C (850F to1560F)

**Plating onto tungsten metallized ceramic.**

1. Alkaline clean. Ultrasonic is preferred)
2. Rinse (ultrasonic is preferred)
3. If the frit has a high glass phase, immerse in a solution of 100 g/L KOH at 100C to boiling for 15 minutes. Omit step 3 if glass content is very low or zero.
4. Rinse
5. Activate tungsten in a solution of 200 g/L potassium ferricyanide and 100 g/L KOH at room temperature to 40C for 20-50 seconds. Too long in the solution can remove too much tungsten.
6. Rinse.
7. Acid dip in sulfamic acid or fluoride containing acid salts.
8. Rinse
9. Catalyze as in step 8 above.
10. Rinse.
11. Dip in 10% HCl, for 30 to 45 seconds.
Electroless nickel plating onto bare ceramic (except AlN)

It is possible to plate directly onto a ceramic surface without first "metallizing" the surface with a "painted on" or screened metal frit. Preparation for plating directly on a ceramic surface takes many forms. The basic requirements are: proper cleaning, a means of developing microporosity in the surface to produce maximum adhesion, a means of making the surface catalytic to an electroless plating solution, and a suitable electroless plating process.

Ideally, a slightly porous surface (where interlocking of plating in the pores with the surface deposit can occur) will produce maximum adhesion. The adhesion is comparable with the bond strength achieved by fired-on metallization coatings. The bond strength diminishes to bonds of 1 to 5 pounds pull (1 inch wide strip), as the porosity becomes less than ideal. Resin and organic and organic coatings as preparation materials have produced bond strength of from 2-15 pounds pull. Porosity in the ceramic surface can be controlled somewhat by the conditions under which the ceramic device is produced. The composition of the ceramic also plays a role in whether or not porosity of a suitable nature can be produced. Where there is a little or no porosity in the ceramic surface, it can sometimes be developed by etching in mixtures containing fluorides. Ninety seven percent alumina is an example of a ceramic that can be etched in fluorides to develop microporosity. Lumina cannot be etched effectively to develop microporosity suitable for plating. An alternate procedure is to immerse the ceramic in a 10% solution of KOH followed, by heat treating at 450°C for 10 minutes.

PLATING ONTO ALUMINA CERAMIC

1. Alkaline clean to remove fingerprints and other soils. Ultrasonic energy aids cleaning and helps remove ceramic fines entrapped in the pores.
2. Rinse (ultrasonic is preferred)
3. Etch in a fluoride-containing solution such as ammonium bifluoride 60-120 g/L or hydrofluoric acid or a mixture of the two, for 2-20 minutes depending on the nature of the ceramic. The addition of 100 g/L NaCl can enhance the adhesion of the subsequent deposit. (see also above for KOH etching using heat treating)
4. Rinse (ultrasonic is preferred)
5. Sensitize in a dilute solution of stannous chloride (10 g/L plus 10 ml/L HCl) 1 to 2 minutes at room temperature.
6. Rinse in DI water.
7. Catalyze in a dilute solution of palladium chloride (1 g/L plus 10 ml/L HCl) 1-2 minutes at room temperature.
8. Rinse in DI water.
10. Rinse
11. Electroplate (optional)
12. Rinse and dry.

PLATING BARIUM TITANATE CERAMIC

1. Alkaline clean (see above method)
2. Rinse (ultrasonic)
3. Etch (see above method)
4. Rinse in DI water (ultrasonic)
5. Sensitize in stannous chloride (see above)
6. Rinse in DI water.
7. Catalyze (see above method)
8. Rinse in DI water.
10. Rinse
11. Electroplate (optional) Use copper, gold, silver or rhodium or as required
12. Rinse and dry.

Note: other ceramic materials have been plated using these processes and modification thereof. Examples or other ceramics plated are: Yttria, stabilized zirconia, lead zirconate, (acetic acid is added to the etching solutions), garnet ceramic, zirconium oxide, lithium niobate and ferrites.

PLATING ONTO BARIUM TITANATE

1. Alkaline clean (Ultrasonic preferred)
2. Rinse
3. Fluoride etch (Ultrasonic preferred)
4. Rinse (Ultrasonic)
5. Sensitize using stannous chloride (see above formula)
6. Rinse in DI water.
7. Catalyze in a dilute solution of palladium chloride 1-2 minutes (see above)
8. Rinse
10. Rinse
11. Electroplate (optional)
12. Rinse and dry.

PLATING ONTO SILVER-FIRED FRIT
1. Mild alkaline clean.
2. Rinse in DI water.
3. Nitric acid dip (10% by vol.) for 15 seconds (Alternate 30 g/L NaCN).
4. Rinse in DI water.
5. Electroless nickel-boron plate. Note: if Nickel phosphorus EN is to be used, a nickel-boron strike may be required to initiate deposition.
6. Rinse in DI water.
7. Electroplate (optional).
8. Rinse and dry.

**PLATING ONTO METALLIZED AlN (aluminum Nitride)**

Note: AlN is sensitive to alkaline solutions, therefore an all acid treatment cycle is required.

1. Acid clean (mild phosphoric acid, or organic acid with a surfactant added).
2. Fluoride etch (see above).
3. Catalyze using 0.1 g/L palladium chloride + 20 ml/L HCl, 30 to 45 seconds.
4. Electroless nickel plate.
5. Rinse and dry.

**CONCLUSIONS**

It is possible to electroless nickel plate onto the usual metallized patterns on ceramic substrates. It is also possible to electroless nickel plate directly onto certain ceramic surfaces with good adhesion, provided that microporosity can be achieved either by etching the ceramic, or by manufacturing and firing process used to create pores in fabricated ceramic substrates using the processes provided in this paper. It is also possible to electroplate over the electroless nickel deposits by the usual methods.

**REFERENCES**